

FIG. 1

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graph LR; 110[PROCESSOR] -- 112 --> 120{DAC}; 120 -- 123 --> 130[LOW PASS FILTER]; 130 -- 134 --> 140[LINE DRIVER]; 140 -- 141 --> 144; 140 -- 142 --> 144;
```

FIG. 2

140

141 142 142 144

212 223

LOW VOLTAGE PORTION BLOCK

BIAS CURRENT GENERATOR

HIGH VOLTAGE PORTION BLOCK

134 210 213 220 230

[illegible]

2/2

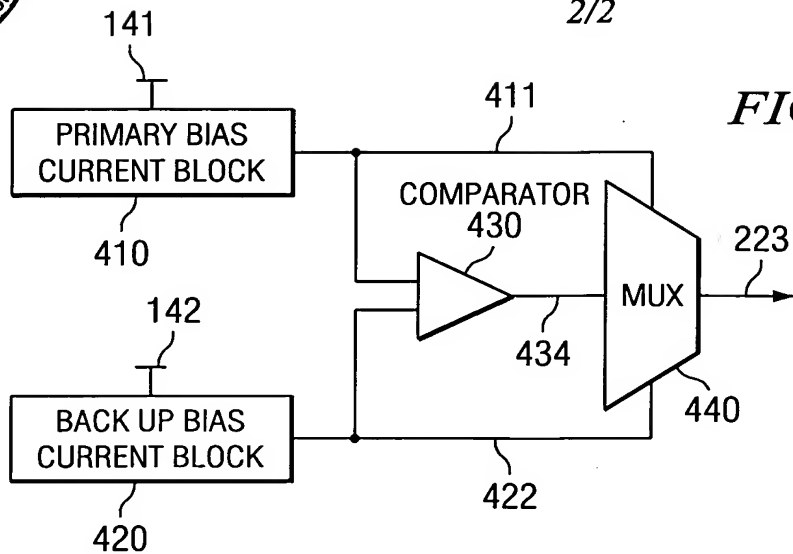


FIG. 4

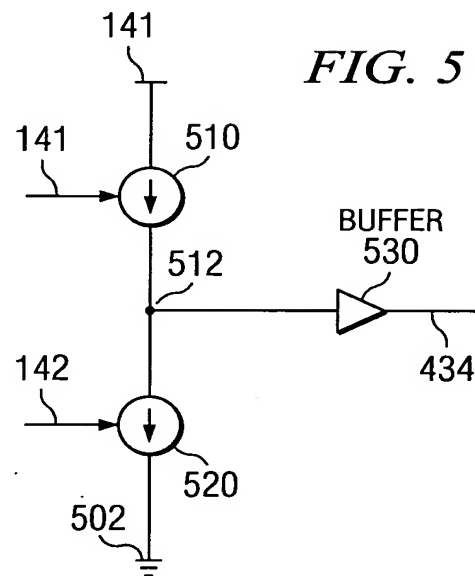


FIG. 5

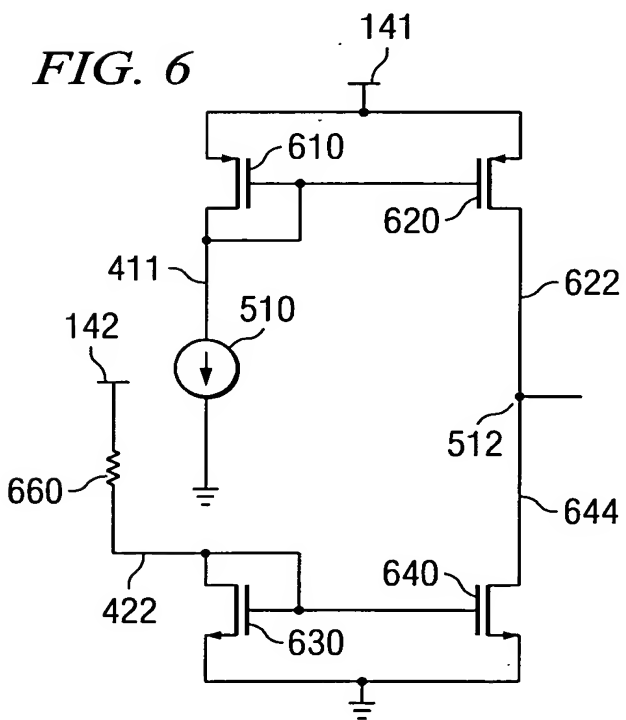


FIG. 6

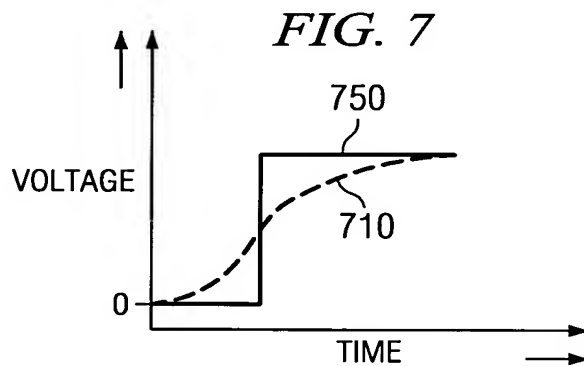


FIG. 7